Digital Logic Design Final Exam Solution

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EE 202 - Introduction to Digital Logic Design
ECE/CS 352 Final Exam May 12, 2002 1 Department of Electrical and Computer Engineering University of Wisconsin - Madison ECE/CS 352 Digital System Fundamentals Final Exam Solution Sunday, May 12, 2002 7:45 AM--9:45AM 1. (20 points) Review problems ... the design to use as few logic gates as possible. Answer: Idle S0 G 0 1 check S1 Q

Digital Logic Design Final Examination
UNC- Charlotte ECGR 2181 - Fall 2009 - Logic Systems Design I Recitation - All Sections: 8:00 - 10:45 F, Woodward 125 ... 9/18/09 - Boolean Algebra, digital gates ; Quiz 5 - 9/25/09 - Minimizing SOP, XNOR/NAND/NOR logic gates; Quiz 6 - 10/2/09 - Minimizing SOP, NAND logic gates, Muxes; ... Exam 1 solution; Spring 2006 - Exam 2 solution ...

Fall 2016 - ECE278: Digital Logic Design - Oakland University
You might find it useful to use a drawing program to draw your logic diagrams for your assignments. I normally use xfig to draw my figures. Here a file containing templates for basic gates in xfig format. Requires an X-windows.

CSE 260 – Introduction to Digital Logic and Computer ...
ENEE244-010x: Digital Logic Design Fall 2015 Final Exam Info The Final Exam will be held on Wednesday, Dec. 16 from 1:30-3:30pm in EGR 1108. It will consist of 9 problems (some with multiple parts). The exam is **cumulative** and will cover material from the entire semester, with emphasis on material since the last exam (Lectures 16-24).

CSE370 Final Exam Solution - courses.cs.washington.edu
Fall 2013 - Workshop: Digital Circuit Design with VHDL; Fall 2013 - ECE238L: Computer Logic Design; Summer 2013 - ECE314: Signals and Systems; Fall 2005 - IEE146: Laboratory of Digital Circuits (in Spanish) Digital Library. DSP/DIP cores; Arithmetic Cores; Fall 2013 - Computer Logic Design (ECE-238L) For VHDL material, see ... FINAL Exam (in ...

ENEE244-010x: Digital Logic Design Fall 2015 Final Exam Info
Evaluation Strategy : Your final grade in this course will be based on seven quizzes (50% total), one mid-term exam (20%) and a comprehensive final exam (30%). We'll drop 2 quizzes with the lowest score. No alternative test arrangements can be made. Graded quizzes and exams will be returned through the distribution center.

EE 110 Practice Problems - Digital Logic - Fall 2008
CSE 260 – Introduction to Digital Logic and Computer Design Jonathan Turner Final Exam Solution 5/7/2014 - 2 - 2. (10 points). Use the Karnaugh map below to find a minimum sum-of-products expression for Σ m(0,1,3,4,5,8,9,12,14). How many simple gates of each type are needed to implement this ...

Digital Logic Design Final Exam
COE/EE 243 Digital Logic Session 44; Page 1/5 Spring 2003 COE/EE 243 Sample Final Exam From Fall 98 Solutions Show your work. Do NOT use a calculator! 1. (9 pts) Complete the following table of equivalent values.

ENEL 353 - Digital Circuits Final Examination
Logic Circuits (630211) Exams . Exams (2019-2020) First Semester: Quizzes . Quiz 1 Solution . Quiz 2 Solution ... Final Exam. Final Exam : Solution . Exams (2018-2019) First Semester: First Exam: First Exam: Solution . Second Exam: Second Exam : Solution . Final Exam: Final ...

ECE/CS 352 Digital System Fundamentals Final Exam Solution
CSE370 Final Exam Solution 1. Combinational Logic (10 points) You are to design a circuit that takes a 4-bit number as input (F8, F4, F2, F1) and generates an output which is 1 if the input number is one of the Fibonacci numbers between 2 and 15 and 0 otherwise.

Logic Circuits (630211) Exams
EECE 256 Digital Logic Design . Section 101/102 Term 1 - 2010/11. Final Exam in SRC A, 3:30-6:00, Tuesday Dec 7 th. Midterm Solution & old final questions posted. Exam covers Chap

Digital Systems Practice Exams - Electrical and Computer ...
Final Exam Review • Combinational Logic Building Blocks: – Decoders, Encoders, Multiplexers, Demultiplexers – Implementing functions using decoders, multiplexers. ... (MUX) is a digital switches which connects data from one of n sources to the output.

CS 151 SQ08 Digital Logic Design
ENEL 353 Final Examination - Fall 2008 Page 5 of 12 (d) [6 marks.] Re-design the circuit in Fig. 2 using only 2-to-1 multiplexers. Use at most seven such multiplexers and no other logic gates.

EE/COE243: Digital Logic - uidaho.edu
EE 202 - Introduction to Digital Logic Design. Fall 2010 Test and Solutions. EE 202 Sample Test 1. EE 202 Sample Test 1 Solution. EE 202 Test 1. EE 202 Test 1 Solution. EE 202 Sample Test 2. EE 202 Sample Test 2 Solution. EE 202 Test 2. EE 202 Test 2 Solution. ... EE 202 Final Exam.

Logic Design Final Exam Flashcards | Quizlet
EECS:1100 Digital Logic Design Dr. Anthony D. Johnson Student name _____ Problem 1 12 points Given is a logic (switching) function F 1 in the decimal list sum-of-minterms representation (1-1). Problem statement On the example of the given logic function F 1 demonstrate an ability to:

UBC EECE 256 - Digital Logic Design
Reconfigurable Computing Research Laboratory (RECRLab), Electrical and Computer Engineering Department, Oakland University, Electrical and Computer Engineering Department, Oakland University

Final Exams Review - University of Waterloo
Logic Design Final Exam study guide by markdbatson includes 50 questions covering vocabulary, terms and more. Quizlet flashcards, activities and games help you improve your grades.

Sample Final Exam Solutions - University of Idaho
EE 110, Digital Logic: Practice Problems. Practice Problems for Exam 1. Solutions to Practice Problems for Exam 1. Practice Problems for Exam 2. Solutions to Practice Problems for Exam 2. Practice Problems for Final Exam. Solutions to Practice Problems for Final Exam

Fall 2013 - ECE238L: Computer Logic Design
Final Exams Review Spring 2011 . Should you have any questions on this review, please contact Arash. [aTabibiazar@uwaterloo.ca] ECE124 Digital Circuits and Systems, Final Review, Spring 2011 Should you have any questions on this review, please contact Arash. ... Design a digital circuit that takes two 4 -bit numbers A and B as input and ...

ECGR2181 - Logic Systems Design I - Exams
Memory and programmable logic, register transfer and computer operations, control logic design. Computer instructions and addressing modes, and design of a CPU input-output communication memory management Practice Exams Digital Design_Spring 2010 Digital Design_Fall 2010 Digital Design Fall 2011 Digital Design Spr 2011 Digital_Fall 2012 Digital ...